REMARKS

This is intended as a full and complete response to the Office Action dated March 25, 2008 (hereinafter "the Office Action") having a shortened statutory period for response set to expire on June 25, 2008.

Claims 1-10, 11-30, and 31-43 were subject to two restriction requirements, from which claims 1-10 were elected with traverse. Non-elected claims 11-43 have been canceled without prejudice. Applicant reserves the right to present such canceled claims in one or more subsequent applications.

Claims 1-10 were presented for examination. Claims 1-10 were rejected as indicated below. Claims 7 and 8 have been canceled without prejudice in favor of the amendment to claim 1. Claims 1 and 4 have been amended. Support for the amendments to the claims may be found in the specification of the above-captioned application, for example at paragraphs [0066] and [0067], as well as FIG. 4A. Further examination and reconsideration are respectfully requested in view of the above-amendment and the following remarks.

The Information Disclosure Statement ("IDS") was not completely considered for reasons outlined in the Office Action. A substitute form 1449A setting forth the U.S. patent applications listed in the prior IDS has been submitted herewith to comply with 37 CFR 1.97, 1.98, and MPEP § 609 as indicated in the Office Action. Note that Applicants have updated the listing to reflect U.S. Patent numbers for those references that have issued since the filing of the original IDS. Accordingly, consideration of the information referred to in the attached substitute form 1449A is respectfully requested. No fee is believed to be due; however the Commissioner is authorized to charge and fee or credit any overpayment which may be required to Deposit Account No. 24-0040.

The declaration was considered defective for reasons indicated in the Office Action. The application data sheet has been revised to clearly identify the address of residence for each inventor, and accordingly a Supplemental Application Data Sheet is submitted herewith.

Claim 4 was rejected under 35 U.S.C. § 112 alleging the rejected claims as being indefinite. Claim 4 has been amended to overcome this rejection.

Claims 1-10 were rejected under 35 U.S.C. § 102(b) alleging the rejected claims as being anticipated by U.S. Patent No. 5,563,891 ("Wang"), and claims 3-10 were rejected under 35 U.S.C. §103(b) alleging the rejected claims as being unpatentable over Wang. Applicant believes that only claims 1 and 2 were to have been rejected under 35 U.S.C. § 102(b) in view of the content in the Office Action. Thus, for purposes of clarity, Applicant will address both rejections simultaneously. With both of these rejections, Applicant respectfully disagrees; however, it is believed that these rejections are now moot in view of the amendments to claim 1 at least for the reasons set forth below.

In Wang, a synchronous elastic buffer 602 in FIG. 3 and 120 in FIG. 6 has a read clock port coupled for receiving a gapped read clock output from logic circuit (AND gate) 645 in FIG. 3 and 145 in FIG. 6. The read pointer 625 in FIG. 3 and 125 in FIG. 6 of Wang has a clock port which receives no clock signal and a count in port which receives the gapped read clock. (Wang at col. 2, lines 47-66, and at col. 8, lines 50-57.)

To provided the gapped read clock, the logic circuit 645/145 in Wang receives a read clock signal from a local oscillator 640 in FIG. 3 and 140 in FIG. 6, a justification signal from justification decision circuit 635 in FIG. 3 and 135 in FIG. 6, and a frame/overhead timing signal from multiplexer 650 in FIG. 3 and 150 in FIG. 6. (Wang at col. 3, lines 53-65, and at col. 8, lines 43-49.) However, the gapped read clock has pulses of varying width, or is jittery. (Wang at col. 3, line 65, to col. 4, line 7.) To address this jitter, Wang has additional and substantial overhead of a random number

threshold generator 155 in FIG. 6. Thus, as indicated in Wang, with a fixed threshold there is substantial jitter in gapped read clock, which, according to Wang, may be reduced by adding the overhead of a dynamically randomly varying threshold signal input to justification decision circuit 135. (Wang at col. 9, line 63, to col. 10, line 25, at FIGS. 8a, 8b, and 8c, and at col. 11, lines 10-35.)

In contrast to Wang, amended claim 1 recites in relevant part that: a controller is configured to controllably activate and deactivate operation of a read pointer by electrically coupling and decoupling, respectively, a clock input of the read pointer for obtaining the read clock; and a control register stores a nominal level as a set fill level of the buffer circuit.

In other words, Wang teaches away from a fixed or set threshold due to jitter. According to Wang, to avoid jitter overhead associated with a gapped read clock, a random or pseudorandom dynamically generated threshold may be added. However, in amended claim 1, a set fill level is claimed, where, by controllably activating and deactivating operation of the read pointer by electrically coupling and decoupling, respectively, a read clock is input to a clock input port of the read pointer.

In the Office Action, it is stated that Wang does not teach disabling a clock input to the read pointer and holding the read address when the amount of data is less than a nominal level. Applicant agrees.

In the Office Action, it is stated with reference to the rejection of claim 6, as well as in part the rejection of claim 3, that it would have been obvious in view of Wang to hold the read address of the read pointer and to disable the read clock input in order to hold the read pointer at a current address. Applicant disagrees with this argument.

Again, it is agreed that Wang does not teach disabling a clock input to the read pointer and holding the read address when the amount of data is less than a nominal level. Furthermore, Wang is not directed at clocking the read pointer. Rather, Wang is directed at incrementing the read pointer with a gapped read clock provided to a count-in port of the read pointer and providing the gapped read clock to a read clock port of the synchronous elastic buffer for synchronous operation.

In short, Wang teaches away from activating and deactivating a read pointer as

claimed in amended claim 1. Thus, Applicant contends that amended claim 1, as well as claims 2-6 and 9-10 which depend from amended base claim 1, would be neither anticipated by, nor obvious in view of, Wang.

Accordingly, it is respectfully submitted that claim 1 should be allowed. Furthermore, it is respectfully submitted that claims 2-6, and 9-10, which depend from an allowable base claim 1, should likewise be allowed.

CONCLUSION

All claims should now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicants' attorney can be reached at Tel: 408-879-4641 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent & Trademark Office on June 12, 2008.
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